In the claims:

Please amend claims 1-12 as follows.

1. (Amended) A fuse circuit for a semiconductor integrated circuit, comprising:

a plurality of fuses; and

a plurality of transmission circuits, each transmission circuit being coupled to a corresponding fuse of the plurality of fuses; each transmission circuit for transferring signals from an input node to an output node in response to a status of the corresponding fuse, the input and output nodes of respective adjacent transmission circuits being coupled such that the transmission circuits are arranged in series.

2. (Amended) The fuse circuit of claim 1, wherein each fuse in the plurality of fuses has an identical fusing status.

3. (Amended) The fuse circuit of claim 1, wherein each of the fuses includes first and second terminals, the first terminal of each being connected to a first power supply voltage.

4. (Amended) The fuse circuit of claim 3, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal coupled to a corresponding input node, an output terminal coupled to a corresponding output node, and a primary control terminal connected to the second terminal of the corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal of the corresponding fuse and the primary control terminal, and having an output terminal connected to the secondary control terminal.

5. (Amended) The fuse circuit of claim 4, wherein the transmission gate includes:

a first conductive transistor having a first electrode connected to the input terminal, a control electrode connected to the second terminal of the corresponding fuse, and a second electrode connected to the output terminal; and

a second conductive transistor having a second electrode connected to the input terminal, a control electrode connected to the output terminal of the inverter, and a first electrode connected to the output terminal.

6. (Amended) The fuse circuit of claim 4, wherein the power supply voltage is applied to the input terminal of a first in the series of the plurality of the transmission gates.

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7. (Amended) The fuse circuit of claim 5, wherein each of the transmission circuits further comprises a resistor having a first terminal that is connected to the control electrode of the first conductive transistor and to the input terminal of the inverter, and having a second terminal that is connected to a second power supply voltage.

8. (Amended) A fuse circuit storing information related to a semiconductor integrated circuit, comprising;

a plurality of fuses each of which has first and second terminals, the first terminal of each being connected to a power supply voltage, the fuses each storing predetermined information relevant to the semiconductor integrated circuit; and

a plurality of transmission circuits, each transmission circuit connected to a second terminal of a corresponding fuse of the plurality of fuses, each transmission circuit transferring an input signal received at an input terminal to an output terminal in response to the predetermined information established by a status of the corresponding fuse,

wherein the transmission circuits are connected in series.

9. (Amended) The fuse circuit of claim 8, wherein the plurality of fuses in combination store one-bit of the predetermined information relevant to the semiconductor integrated circuit.

10. (Amended) The fuse circuit of claim 8, wherein each of the transmission circuits comprises:

a transmission gate having an input terminal, an output terminal, a primary control terminal connected to the second terminal of a corresponding fuse, and a secondary control terminal; and

an inverter having an input terminal connected to the second terminal of the corresponding fuse and the primary control terminal, and an output terminal connected to the secondary control terminal.

11. (Amended) The fuse circuit of claim 10, wherein the transmission gate includes:

a NMOS transistor having a drain connected to the input terminal, a gate connected to the second terminal of the corresponding fuse, and a source connected to the output terminal; and

a PMOS transistor having a source connected to the input terminal, a gate connected to the output terminal of the inverter, and a drain connected to the output terminal.

12. (Amended) The fuse circuit of claim 11, wherein each of the transmission circuits further comprises a resistor having a first terminal that is connected to the control electrode of the NMOS transistor and the input terminal of the inverter, and having a second terminal that is connected to the power supply voltage.